Abstract

For the past 40 years, relentless focus on Moore's Law transistor scaling has provided ever-increasing transistor performance and density. In order to continue the technology scaling beyond 22nm node, it is clear that conventional bulk-MOSFET needs to be replaced by new device architectures, most promising being the Multiple-Gate MOSFETs (MuGFET). Intel in mid 2011 announced the use of bulk Tri-Gate FinFETs in 22nm high volume logic process for its next-gen IvyBridge Microprocessor. It is expected that soon other semiconductor companies will also adopt the MuGFET devices. As like bulk-MOSFET, an accurate and physical compact model is important for MuGFET based circuit design.

Compact modeling effort for MuGFET started in late nineties with planar double gate MOSFET (DGFET), as it is the simplest structure that one can conceive for MuGFET devices. The models so far proposed for DG MOSFETs are applicable for common gate symmetric DG (SDG) MOSFETs where both the gates have equal oxide thicknesses. However, for practical devices at nanoscale regime, there will always be some amount of asymmetry between the gate oxide thicknesses due to process variations and uncertainties, which can affect device performance significantly. At the same time, Independently controlled DG (IDG) MOSFETs have gained tremendous attention owing to its ability to modulate threshold voltage and transconductance dynamically. Due to the asymmetric nature of the electrostatic, developing efficient compact models for asymmetric/independent DG MOSFET is a daunting task. In this thesis effort has been put to provide some solutions to this challenge.

We propose simple surface-potential based compact terminal charge models, applicable

for Asymmetric Double gate MOSFETs (ADG) in two configurations 1) Common-gate 2) Independent-gate. The charge model proposed for the common-gate ADG (CDG) MOSFET is seamless between the symmetric and asymmetric devices and utilizes the unique so-far-unexplored quasi-linear relationship between the surface potentials along the channel. In this model, the terminal charges could be computed by basic arithmetic operations from the surface potentials and applied biases, and can be easily implemented in any circuit simulator and extendable to short-channel devices. The charge model proposed for independent ADG (IDG) MOSFET is based on a novel piecewise linearization technique of surface potential along the channel. We show that the conventional "charge linearization techniques that have been used over the years in advanced compact models for bulk and double-gate (DG) MOSFETs are accurate only when the channel is fully hyperbolic in nature or the effective gate voltages are same. For other bias conditions, it leads to significant error in terminal charge computation. We demonstrate that the amount of nonlinearity that prevails between the surface potentials along the channel for a particular bias condition actually dictates if the conventional charge linearization technique could be applied or not. We propose a piecewise linearization technique that segments the channel into multiple sections where in each section, the assumption of quasi-linear relationship between the surface potentials remains valid. The cumulative sum of the terminal charges obtained for each of these channel sections yield terminal charges of the IDG device.

We next present our work on modeling the non-ideal scenarios like presence of body doping in CDG devices and the non-planar devices like Tri-gate FinFETs. For a fully depleted channel, a simple technique to include body doping term in our charge model for CDG devices, using a perturbation on the effective gate voltage and correction to the coupling factor, is proposed. We present our study on the possibility of mapping a non-planar Tri-gate FinFET onto a planar DG model. In this framework, we demonstrate that, except for the case of large or tall devices, the generic mapping parameters become bias-dependent and an accurate bias-independent model valid for geometries is not possible.

An efficient and robust "Root Bracketing Method" based algorithm for computation of surface potential in IDG MOSFET, where the conventional Newton-Raphson based techniques are inefficient due to the presence of singularity and discontinuity in input-voltage equations, is presented. In case of small asymmetry for a CDG devices, a simple physics based perturbation technique to compute the surface potential with computational complexity of the same order of an SDG device is presented next. All the models proposed show excellent agreement with numerical and Technology Computer-Aided Design (TCAD) simulations for all wide range of bias conditions and geometries. The models are implemented in a professional circuit simulator through Verilog-A, and simulation examples for different circuits verify good model convergence.