Abstract

There has been a huge rise in interest in the design of energy efficient wireless sensor networks (WSN) and body area networks (BAN) with the advent of many new applications over the last few decades. The number of sensor nodes in these applications has also increased tremendously in the order of few hundreds in recent years.

A typical sensor node in a WSN consists of circuits like RF transceivers, micro-controllers or DSP, ADCs, sensors, and power supply circuits. The RF transmitter and receiver circuits mainly the frequency synthesizers (synthesis of RF carrier and local oscillator signals in transceivers) consume a significant percentage of its total power due to its high frequency of operation. A charge-pump phase locked loop (CP-PLL) is the most commonly used frequency synthesizer architecture in these applications.

The growing demands of WSN applications, such as low power consumption, larger number of sensor nodes, single chip solution, and longer duration operation presents several design challenges for these transmitter and frequency synthesizer circuits in these applications and a few are listed below,

- Low power frequency synthesizer and transmitter designs with better spectral performance is essential for an energy efficient operation of these applications.
- The spurious tones in the frequency synthesizer output will mix the interference signals from nearby sensor nodes and from other interference sources present nearby, to degrade the wireless transmitter and receiver performance [1]. With the increased density of sensor nodes (more number of in-band interference sources) and degraded performance of analog circuits in the nano-meter CMOS process technologies, the spur reduction techniques are essential to improve the performance of frequency synthesizers in these applications.
- A single chip solution of sensor nodes with its analog and digital circuits integrated on the same die is preferred for its low power, low cost, and reduced size implementation. However, the parasitic interactions between these analog and digital sub-systems integrated on a common substrate, degrade the spectral performance of frequency synthesizers in these implementations [2]. Therefore, techniques to improve the mixed signal integration performance of these circuits are in great demand.

In this thesis, we present a custom designed energy efficient 2.4 GHz BFSK/ASK transmitter architecture using a low power frequency synthesizer design technique taking advantage of the CMOS technology scaling benefits. Furthermore, a few design guidelines and solutions to improve the spectral performance of frequency synthesizer circuits and in-turn the performance of transmitters are also presented. The target application being short distance, low power, and battery operated wireless communication applications.

The contributions in this thesis are,

Spectral performance improvement techniques

- The CP mismatch current is a dominant source of reference spurs in the nanometer CMOS PLL implementations due to its worsened channel length modulation effect [3]. In this work, we present a CP mismatch current calibration technique using an adaptive body bias tuning of its PMOS transistors.

  Chip prototype of 2.4 GHz CP-PLL with the proposed CP calibration technique was fabricated in UMC 0.13 μm CMOS process. Measurements show a CP mismatch current of less than 0.3 μA (0.55 %) using the proposed calibration technique over the VCO control voltage range 0.3 to 1 V. The closed loop PLL measurements using the proposed technique exhibited a $\simeq$9 dB reduction in the reference spur levels across the PLL output frequency range 2.4 - 2.5 GHz.

- The parasitic interactions between analog and digital circuits through the common substrate severely affects the performance of CP-PLLs. In this work, we experimentally demonstrate the effect of periodic switching noise generated from the digital buffers on the performance of charge-pump PLLs. The sensitivity of PLL performance metrics such as output spur level, phase noise, and output jitter are monitored against the variations in the properties of a noise injector digital signal.

  Measurements from a 500 MHz CP-PLL shows that the pulsed noise injection with the duty cycle of noise injector signal reduced from 50% to 20%, resulted in a 12.53 dB reduction in its output spur level and a 107 ps reduction in its Pk-Pk deterministic period jitter performance.

Low power circuit techniques

- A low power frequency synthesizer design using a digital frequency multiplication technique is presented. The proposed frequency multiply by 3 digital

edge combiner design having a very few logic gates, demonstrated a significant reduction in the power consumption of frequency synthesizer circuits, with an acceptable spectral performance suitable for these relaxed performance applications. A few design guidelines and techniques to further improve its spectral performance are also discussed and validated through simulations.

Chip prototypes of 2.4 GHz CP-PLLs with and without digital frequency multiplier circuits are fabricated in UMC 0.13 μm CMOS process. The 2.4 GHz CP-PLL using the proposed digital frequency multiplication technique (10.7 mW) consumed a much reduced power compared to a conventional implementation (20.3 mW).

- A custom designed, energy efficient 2.4 GHz BFSK/ASK transmitter architecture using the proposed low power frequency synthesizer design technique is presented. The transmitter uses a class-D power amplifier to drive the 50Ω antenna load. Spur reduction techniques in frequency synthesizers are also used to improve the spectral performance of the transmitter.

  A chip prototype of the proposed transmitter architecture was implemented in UMC 0.13 μm CMOS process. The transmitter consume 14 mA current from a 1.3 V supply voltage and achieve improved energy efficiencies of 0.91 nJ/bit and 6.1 nJ/bit for ASK and BFSK modulations with data rates 20Mb/s & 3Mb/s respectively.